Patent Claims

1. Process measuring device comprising: A first processor (21), which performs a measured value processing in first processing cycles with a first algorithm; and a second processor (25), which is responsible for coordination and/or communication tasks, wherein, additionally, the second processor (25), in time intervals, which are greater than the first processing cycle, reads a control data set from the first processor (21), and, on the basis of the control data set, executes the first algorithm, in order to verify correct functioning of the first processor.

2. Process measuring device as claimed in claim 1, wherein the control data set contains raw measured values of a sensor and state variables, as well as associated result values calculated therefrom by the first processor.

3. Process measuring device as claimed in claim 1 or 2, wherein the verifying occurs by direct comparison of the result read from the first processor (21) with the result of the performing of the first algorithm by the second processor (25).

4. Process measuring device as claimed in one of claims 1 to 3, wherein the second processor includes a program memory and the program memory is regularly verified by means of a test sum or a CRC.

5. Process measuring device as claimed in one of claims 1 to 4, wherein the second processor further includes a write/read memory,

which the second processor can regularly check for static errors by means of test pattern.

6. Process measuring device as claimed in one of the claims 1 to 5, wherein the second processor includes a write/read memory, which the second processor can regularly check for static errors by means of test algorithm.

7. Process measuring device as claimed in one of the claims 1 to 6, wherein the second processor compares and verifies data in the program memory of the first processor with a locally mirrored, memory range.

8. Process measuring device as claimed in one of the claims 1 to 7, wherein the second processor verifies known constants in the data memory of the first processor by comparison with locally mirrored values.

9. Process measuring device as claimed in one of the claims 1 to 8, wherein the second processor regularly verifies configuration registers of the first processor by comparison with locally mirrored values.

10. Process measuring device as claimed in one of the claims 1 to 9, wherein the process measuring device includes a 4..20 mA, two-wire interface, and wherein a watchdog-circuit checks the functioning of the second processor and an associated clock, and, in the case of error, signals an error via the 4..20 mA signal current, independently of the first processor (21) and the second processor (25).